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15EC663

## Sixth Semester B.E. Degree Examination, June/July 2019 Digital System Design using Verilog

Time: 3 hrs.

Max. Marks: 80

**Note: Answer any FIVE full questions, choosing  
ONE full question from each module.**

### Module-1

- 1
  - a. Define the terms setup time, hold time and clock to output time of a flip-flop and what are the constraints imposed by these parameter on the circuit operations. (05 Marks)
  - b. Develop verilog module for 7 segment decoder. Include an additional input 'blank' that overrides the BCD input and causes all segments not to be lit. (06 Marks)
  - c. Explain functional verification and formal verification for a verilog module (05 Marks)

OR

- 2
  - a. What are the effects of capacitive loading and propagation delay on signal transitions between logic levels? (08 Marks)
  - b. Develop verilog module for 4 : 1 MUX. (04 Marks)
  - c. Explain general view of digital system with data path control section. (04 Marks)

### Module-2

- 3
  - a. Design a 64k × 8 bit composite memory using four 16k × 8 bit components and also explain how memory components with tristate data outputs simplify the construction of larger memories. (08 Marks)
  - b. Explain asynchronous static RAM with timing diagrams. (08 Marks)

OR

- 4
  - a. Write a note on multiport memories. (08 Marks)
  - b. Explain error detection and correction with one example. (08 Marks)

### Module-3

- 5
  - a. Explain different types of PCB design. (05 Marks)
  - b. Explain implementation fabrics for digital system based on integrated circuit. (07 Marks)
  - c. What are EMI and cross talk? (04 Marks)

OR

- 6
  - a. Briefly explain programmable array logic. (08 Marks)
  - b. Explain signal integrity issue in PCB design and also explain measures to reduce these issues. (08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

**Module-4**

- 7 a. Explain the serial transmission of 64 bit data within clock domain with timing diagram. (08 Marks)
- b. Explain the following serial interface standards for connecting I/O devices. (08 Marks)
- i) RS232 ii) Fire wire.

**OR**

- 8 a. Explain any 4 analog sensors. (08 Marks)
- b. Explain the concept of multiplexed buses (08 Marks)

**Module-5**

- 9 a. Explain logical partitioning and physical partitioning of a transport monitoring system. (08 Marks)
- b. Explain fault model and fault simulation. (08 Marks)

**OR**

- 10 a. Explain 4 bit LFSR and CFSR for generating pseudorandom test vectors. (08 Marks)
- b. Explain briefly area, power and timing optimization in digital circuits. (08 Marks)

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